Design and Analysis of 4x4 bit various Multiplier Using Look-up table and implementation in FIR Filter

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***Abstract*— In the comparison of 4 x 4 multiplier according to time, area, and speed, Look-Up Tables (LUTs) are used to meet high speed and low power requirements, which are essential in VLSI. In the implementation of Wallace tree, Booth, , array multipliers, to identify the most efficient one considering all VLSI aspects. Wallace tree multipliers and Booth multipliers are more effective than array multipliers in terms of delay and power consumption, which makes them more appropriate in area while sacrificing in speed.. But the Wallace tree multiplier is more suitable for FIR filters than other filters. The Xilinx ISE tool is used to implement Verilog code for generating schematic views of the multipliers, highlighting time, speed, and area characteristics.The FIR filter is implemented using MATLAB software.**

***Keywords*—Wallace tree multiplier Booth multiplier, Array multiplier, FIR Filter.**

I. Introduction

A wide range of DSP applications usually call for efficient multiplication procedures. In this article, the creation and analysis of a 4x4 multiplier for use in a FIR filter are done using Look-Up Table (LUT) techniques. Multiplication is the foundation of many digital signal processing techniques, and choosing the best multiplier architecture has a big impact upon the system's overall efficiency. The analysis involves examining several multiplier designs, assessing their capabilities, and employing the LUT approach to select the optimal 4x4 multiplier structure. The effectiveness and efficiency of the chosen multiplier design are then evaluated in practical digital signal processing applications by implementing it inside a FIR filter. The purpose of this work was to improve signal processing methods by shedding light on the viability and efficacy of LUT-based multiplier within FIR filter.

II. MULTIPLIERS

Multiplication techniques are vital to digital signal processing because they are important in terms of both speed and efficacy. This study uses Look-Up Table (LUT) methodologies to analyse the design and analysis of a 4x4 multiplier that is especially intended to work smoothly into a Finite Impulse Response (FIR) filter. Multiplication is a crucial operation through the analysis of signals methods that significantly affects the system's performance in general. Three different multiplier architectures are explored in the study: Wallace's intrinsic benefits in power consumption and time delay set it apart from other explored systems.. Thus, the goal of this study is to determine an ideal 4x4 multiplier design using Look-Up Table methods. The selected The next step is to install multiplier structure within a FIR filter in order to evaluate its effectiveness and suitability for applications involving signal processing. This work aims to shed light on the suitability and efficacy of LUT-based multipliers at FIR filter applications, perhaps contributing to advancements at digital signal processing methodologies. A wallace tree multiplier with minimal power and latency has been extracted from the references. A quick and space-saving method for high-operand multiplication is provided by the Wallace Tree Algorithms which is extensively used in contemporary DSP applications. Partial product addition operations add difficulty and time, especially for larger bits of multiplication. This communication describes several strategies used in the circuitry for partial product addition to maximise the wallace multiplier's area, delay, and speed. [2]. An recommended sixteen-bit wallace multiplier is implemented using a carry select adder (csa) and a binary to excess -1 converter (bec) adder. A comparative study shows that when using csla instead of bec, the wallace multiplier has a smaller latency. [3].The shift and add techniques are *applied in the suggested method to produce an high-speed, low-power multiplier. The research investigates the implementation of braun and wallace multipliers using the cadence (encounter) rtl compiler, including test circuit construction and simulation for every block in the multiplier architecture. [10].Area optimisation and power consumption reduction are the two main factors to be taken into account while designing and executing a DSP processors. The core component of a DSP processing is a Finite Impulse Response Filter, which is made up of multiplier, flip-flop, and adder blocks. Performance of the FIR Filter is mostly dependent on the multiplier, which is the slowest block among them. [11]. The quick co-processors, DSP chips, and graphics processors of today have developed to meet consumer demand for area-efficient and high-speed multipliers. The concepts presented range from small, high- performance shift and add multipliers to massive, low-performance array and tree multipliers. Large amounts of silicon are needed for the operation of conventional linear array multipliers. Although the linkages among the trees are more complicated and less regular, topologies of trees now outperform linear arrays in terms of performance. Many multiplier designs have been constructed and presented in papers in the last few years.. A multiplier is an essential piece of hardware for the majority of high-performance digital systems, including digital signal processors including microprocessors. Many researchers have replaced inefficient multipliers with more effective ones because of recent technological advancements. The primary goal of this work is to provide reduced power usage without increasing the area of silicon.*

A. *Wallace tree Multiplier*

Digital circuits and processors employ the Wallace Tree multiplier, a fast and effective hardware multiplier. It is intended to multiply two binary values by dividing the operation into a number of effective partial products, which are then combined. This multiplier design, named for its creator, Charles W. Wallace, is well-known for its quick binary multiplication capabilities, which make it an essential part of many contemporary processor and digital signal processing applications. The Wallace tree is employed to reduce the quantity of incomplete products required to be incorporated into the two ultimate intermediate outcomes. Multiplying two unsigned values is the basic operation of a Wallace tree. In 1964, Chris, an Australian computer scientist, designed the Wallace tree multiplier is a useful piece of hardware to produce a digital circuit that could multiply two numbers.

One parallel multiplier architecture that is well-known for its multiplication efficiency is the Wallace tree multiplier. Three steps are involved in the process of multiplication:

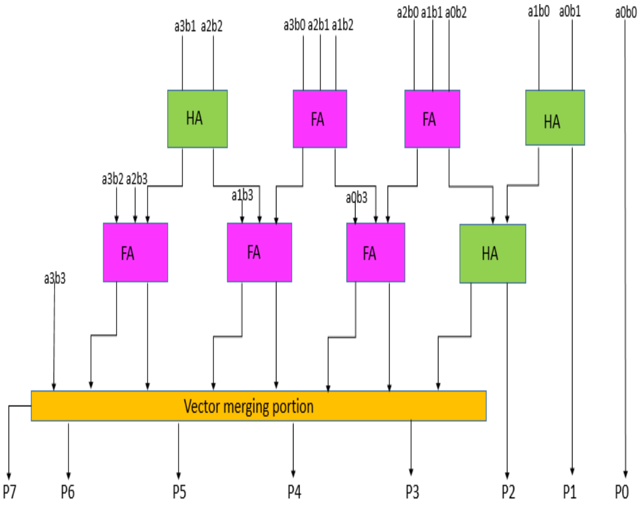


Fig1:4x4 wallace tree multiplier Architecture

Formation

1. *Partial Product Generation Stage: This is the initial stage of the binary multiplier process. These are the terms in between that are produced according to the multiplier value.The partial product row is also "0" (zero) if the multiplier bit is "0" (zero), and we can duplicate the multiplicand exactly if it is "1" (one). The example above shows how, beginning with the second bit of multiplication, each partial product row is pushed one unit to the left. Therefore, the multiplier's speed and performance are determined by the adder's performance, which is the multiplier's central component. To obtain better performance, the multiplier needs to be pipelined.*
2. *The matrix reduction of a two-row partial product. Reducing this reduction stage'slatency is crucial to the total multiplication process's speed. Here, the initially generated partial products undergo rearrangement, and each reduction stage involves grouping rows into sets of three. Rows that are not includedin these sets are moved straight, unaltered, tothe following phase.*

3. *The final product output is obtained by summing these two rows[5].*

Using a 4x4 Wallace Tree multiplier, a specialised Wallace Tree multiplier architecture, is an efficient method of multiplexing two 4-bit binary values. It applies the same concepts as the general Wallace Tree multiplier even though it was specifically intended for 4-bit inputs. To obtain the ultimate 8-bit result, this approachfirst divides the multiplication into a series of smaller, overlapping 4-bit partial products. After that, these are merged usinga number of adders.Digital *systems that frequently need to do 4-bit multiplication operations, including many DSP and arithmetic applications, frequently use the 4x4 Wallace Tree multiplier.*

B. Array Multiplier

It operates by breaking down a binary multiply of two to an array or matrix of periodic bit-wise operations for addition and multiplication Multiply each bit in a single operand with each bit of the other integer to get the final result .

They provide a quick and efficient way of multiplying binary values, but larger operands need more complex circuitry,which is why they are commonly used inside arithmetic units , digital processors By multiplying each individual bit of one 4-bit input by each one of the second 4-bit operand, this design generates a 4x4 grid of unique multiplication operations. A 4x4 array multiplier is widely used in digital devices wherein 4-bit multiplying operations were popular because it provides an easy-to- use and reliable method of doing binary multiplication.

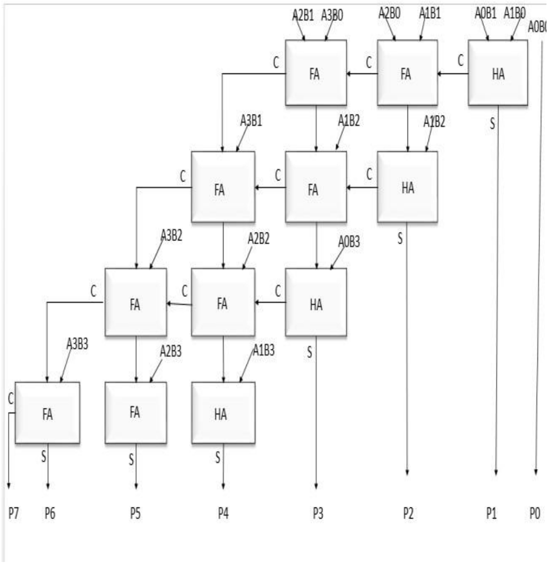


Fig2:4x4 Array multiplier Architecture

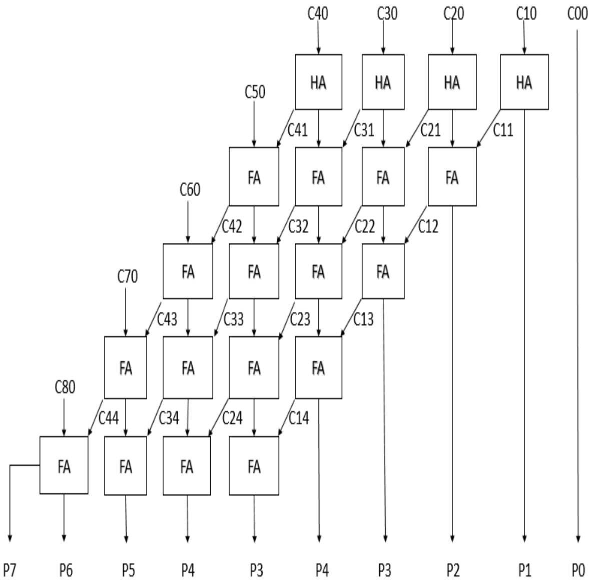
The array multiplier, that's popular for being user-friendly and for using the add-and-shift approach, is the focus of this work. This multiplier analyzes the multiplier bits and produces partial products through a sequence of add and shift actions. Since row-by-row addition is the approach employed, an adder must figure out how much part products and carry combos add up to. [9]. That multiplier is the standard one. Here, the same procedures used for standard multiplication are employed. The foundation of it is the shift-and-add algorithm.

A four- by-four multiplier uses sixteen AND gates, four half adders, eight full adders, and twelve total adders. [2]. Fig. 2 shows that the multiplicand has the bits A0, A1, A2, and A3, along with the multiplier contains the bits B0, B1, B2, and B3. The output bits are p0, p1, p2, p3, p4, p5, p6, and p7. Its structure is regular. Although it is simpler to implement, it uses more energy. A large chip area was the result of using several digital gates. Based on various techniques, different multipliers are built to further reduce power dissipation and propagation delay.

c. ***Booth multiplier***

The hardware-based technique and architecture known as the Booth multiplier, after its creator Andrew D. Booth, is utilized in digital circuits and processors for effective binary multiplication. By embedding patterns in the operands and then employing a series of partial products and additions, the Booth multiplier minimizes the amount of required addition operations in contrast to conventional multiplication techniques that carry out a complete array of binary adds. This approach was more efficient because it involves less additions overall when multiplying large binary numbers. Booth multipliers are widely used in digital arithmetic units and modern. processors, where rapidity and efficacy is vital for complex calculations.

A comparative analysis of the area, delay, or accuracy of both the Booth multiplier with Wallace tree is conducted. Investigates an improved Booth recoder using radix-4 reduction and an effective design in the context to add-multiply operations. Area and critical route calculations are included in the evaluation, which emphasizes this scheme as an exceptionally effective method[7].



. Fig3: 4x4 Booth Multiplier Architecture

A special version of the conventional Booth multiplier architecture designed for 4-bit binary data is called a 4x4 Booth multiplier. With the use of pattern encoding for the operands and a series of partial products and improvements, the Booth approach is able to efficiently combine two 4-bit binary operands. In contrast, a 4x4 Booth multiplier multiplies binary numbers more efficiently by using 4-bit binary integers, thereby decreasing the number of addition operations required. These multipliers are frequently employed in digital systems wherein 4-bit multiplication operations are prevalent to boost speed as well as effectiveness in arithmetic and processing tasks to include LUT-based multipliers in FIR filter designs in order to enhance digital signal processing. It strikes a compromise among hardware complexity and efficiency by choosing effective multiplier designs, carrying out thorough simulations, and putting resource-efficient techniques into practice. The end product is a powerful FIR filter that successfully manages resource use while meeting demanding specifications by utilizing LUT-based multipliers.Multipliers are used in numerous applications including digital signal processing as well as other areas. In an attempt to increase performance, several scholars have concentrated primarily on design issues as a result of recent technical advancements. Several design goals include reduced area, high speed, precision, low power consumption, and regular layout. Multiplexers, adders, and MAC are just a few of the computational blocks found in DSP processors. Compared to earlier iterations, these blocks operate and execute at a faster pace. Two aspects affect multiplier execution speed: multiplier architecture and semiconductor technology. The fundamental component of digital multiplexers are adders, which are used to make a sequence of repeated adds. Increasing the adder's operation speed is necessary to speed up the multiplier action.

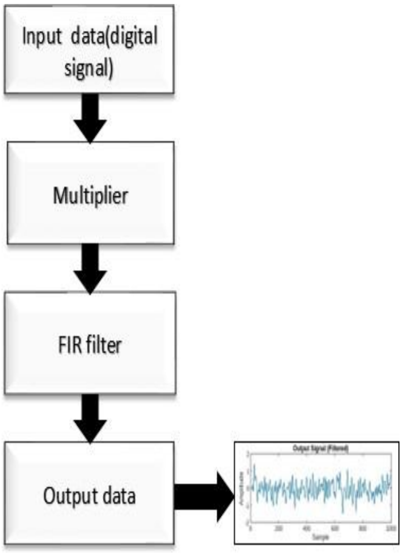


Fig4: work flow of multipliers

They serve as fundamental components in Multiply Accumulate Circuits (MAC) , the core of digital signal processors. The current result is added to the prior MAC result by the MAC, which multiplies two input operands. Reduced depth, lower power consumption, and smaller area multipliers are crucial for digital filter applications such as Finite Impulse Response (FIR) and help achieve high-performance arithmetic in digital systems[6].

III. Stimulation and Result

A. 4x4 Wallace tree multiplier

View of the 4x4 Wallace tree multiplier's RTL schematic.

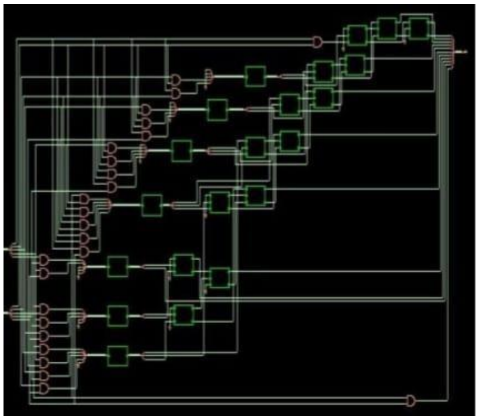
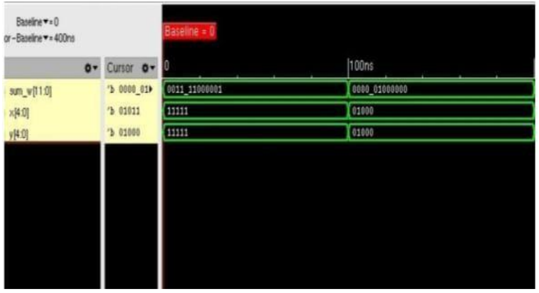


Fig5:(4x4 Wallace tree multiplier RTL view)

The RTL schematic perspective of a 4x4 Wallace tree multiplier is displayed above(Fig.5).



```
sum_w[11:0]  'b 0000_01▸  0011_11000001  0000_01000000
x[4:0]       'b 01011     11111          01000
y[4:0]       'b 01000     11111          01000
```

Fig6:(4x4 Wallace tree multiplier output)

B. 4x4 Array multiplier

RTL schematic view of 4x4 Array multiplier.

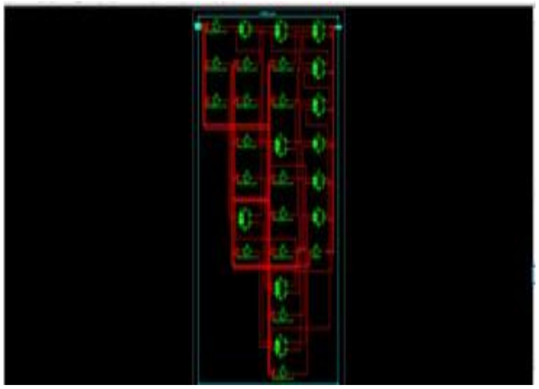


Fig. 7. (4x4 Array multiplier RTL view)

The 4x4 Array multiplier's RTL schematic view is displayed above (Fig. 7). The stimulation of the 4x4 Array multiplier's output (Fig8)

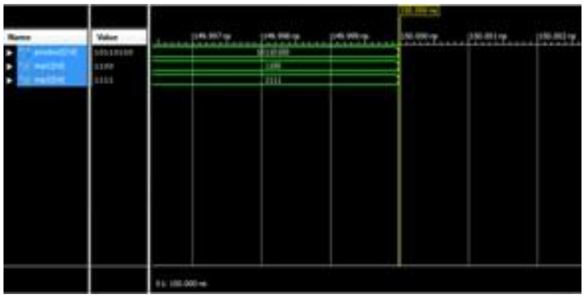


Fig8:(4x4 Array multiplier output)

C. 4x4 Booth multiplier

RTL schematic view of 4x4 Booth multiplier.

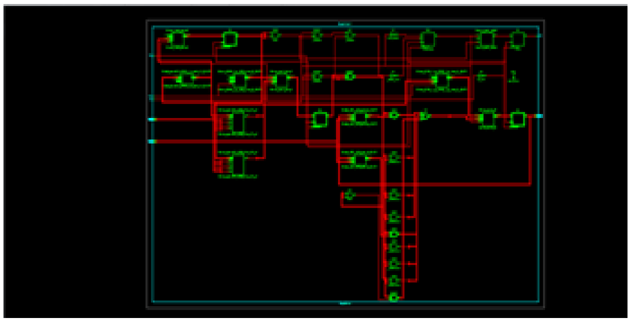


Fig9:(4x4 Booth multiplier RTL view)

The above (Fig9) shows the RTL schematic view of the 4x4 Booth multiplier. The output stimulation of 4x4 Booth multiplier (Fig10)

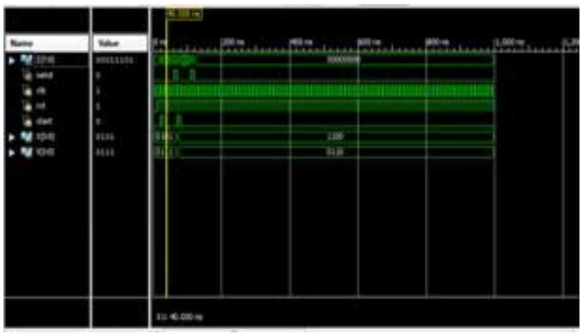


Fig10:(4x4 Booth multiplier output)

Multiplier	Time Delay(ns)	Area(mm^2)	Power consumption (w)
Wallace tree multiplier	**66**	**3.5**	**0.6**
Array multiplier	**89**	**4.5**	**0.9**
Booth multiplier	**78**	**4**	**0.8**

Table.1 COMPARISONS OF PERFORMANCE PARAMETERS OF VARIOUS MULTIPLIERS

The complete performance specifications of the 4x4 bit wallace tree multiplier, array multiplier, and booth multiplier are provided in the preceding table 1.

D.BAR CHART ANALYSIS

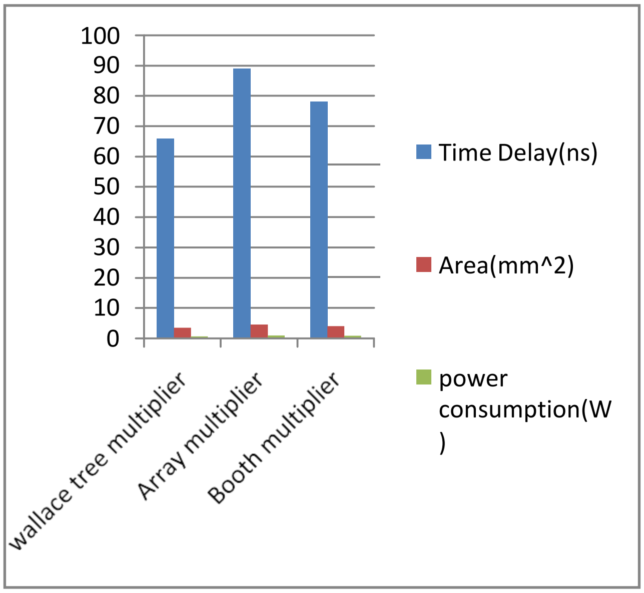


Fig11:(bar chart for multipliers)

The above bar chart Fig.11 shows the graphical representation of performance parameters for wallace tree multipliers,Array multiplier, Booth multiplier.

Then implemented the best multiplier in the fir filter .we get Fig.12.

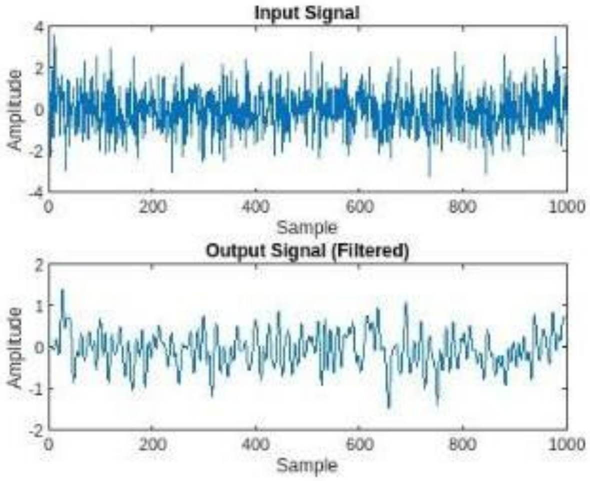


Fig12:(output view of fir filter)

The above figure shows the fir filter by using the wallace tree multiplier. The input signal has some distortion by using this particular multiplier we can get an filtered output faster.

CONCLUSION

In terms of performance parameters, the Wallace tree multiplier is more effective and better suited for FIR (finite impulse response) filter applications when compared to other 4x4 bit multipliers based on time, area, and speed, using look-up tables to meet high-speed requirements and low power consumption. Booth multipliers, on the other hand, are also effective, but they are used in high-speed, low-power applications. Thus, based on the analysis of area, time, and power consumption using the Xilinx ISE tool, the Wallace tree multiplier is more appropriate for this application. Among these three multipliers, the Wallace tree multiplier had the least amount of time lag and the least amount of power usage, whereas the Booth multiplier showed higher power consumption and time delays than the Wallace tree. Another multiplier that is compared is the array multiplier, which displayed the longest duration and is unsuitable for this application.

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